UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,807	02/27/2004	Ming-Sheng Tung	251613-1020	7848

24504 7590 05/04/2005

THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
NOVACEK, CHRISTY L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,807	TUNG ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the communication filed February 27, 2004.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-10, 12-14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Zheng et al. (US 6,762,085).

Regarding claim 1, Zheng discloses forming a gate including a gate dielectric layer (2) and a conductive layer (3) on a substrate (1), forming a liner (4a/4b/4c) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a source/drain region (8/9/12/13) outside of the gate in the substrate, etching the liner to reduce a thickness of the liner, and performing a second-type ion implantation to form a halo region (7/11) surrounding the source/drain region (Fig. 1-7; col. 2, ln. 43 – col. 4, ln. 48).

Regarding claims 2 and 9, Zheng discloses that the conductive layer includes polysilicon (col. 2, ln. 56-65).

Regarding claims 3 and 10, Zheng discloses that the conductive layer includes a silicide layer on the polysilicon layer (col. 2, ln. 56-65).

Regarding claims 5 and 12, Zheng discloses that the first-type ions can be N-type ions and the second-type ions can be P-type ions (col. 3, ln. 41 – col. 4, ln. 15).

Regarding claims 6 and 13, Zheng discloses that the first-type ions can be P-type ions and the second-type ions can be N-type ions (col. 4, ln. 16-51).

Regarding claims 7 and 14, Zheng discloses that the gate has a cap layer (4a/4b/4c) on the conductive layer (Fig. 2-7).

Regarding claim 8, Zheng discloses forming a gate including a gate dielectric layer (2) and a conductive layer (3) on a substrate (1), forming a liner (4a/4b/4c) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a source/drain region (8/9/12/13) outside of the gate in the substrate, etching the liner on one sidewall of the gate to reduce a thickness of the liner, and performing a second-type ion implantation to form a halo region (7/11) surrounding one of the source/drain regions adjacent to the etching side (Fig. 1-7; col. 2, ln. 43 – col. 4, ln. 48).

Regarding claim 16, Zheng discloses forming a mask layer covering another side of the gate prior to etching the liner (col. 2, ln. 61-67).

Regarding claim 17, Zheng discloses that the mask layer is a photoresist layer (col. 2, ln. 61-67).

Claims 1-3, 5-10, 12-14, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Roy et al. (US 6,777,298).

Regarding claim 1, Roy discloses forming a gate including a gate dielectric layer (14) and a conductive layer (16) on a substrate, forming a liner (18/20) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a

source/drain region (24a/24b) outside of the gate in the substrate, etching the liner to reduce a thickness of the liner, and performing a second-type ion implantation to form a halo region (28a/28b) surrounding the source/drain region (Fig. 1-6; col. 2, ln. 47 – col. 4, ln. 32).

Regarding claims 2 and 9, Roy discloses that the conductive layer includes polysilicon (col. 2, ln. 56-59).

Regarding claims 3 and 10, Roy discloses that the conductive layer includes a silicide layer (32b) on the polysilicon layer (col. 3, ln. 59-66).

Regarding claims 5 and 12, Roy discloses that the first-type ions can be N-type ions and the second-type ions can be P-type ions (col. 2, ln. 47 – col. 4, ln. 32).

Regarding claims 6 and 13, Zheng discloses that the first-type ions can be P-type ions and the second-type ions can be N-type ions (col. 2, ln. 47 – col. 4, ln. 32).

Regarding claims 7 and 14, Zheng discloses that the gate has a cap layer (18) on the conductive layer (Fig. 1-4).

Regarding claim 8, Roy discloses forming a gate including a gate dielectric layer (14) and a conductive layer (16) on a substrate, forming a liner (18/20) on the sidewall of the gate, performing a first-type ion implantation, using the gate and the liner as a mask to form a source/drain region (24a/24b) outside of the gate in the substrate, etching the liner on one sidewall of the gate to reduce a thickness of the liner, and performing a second-type ion implantation to form a halo region (28a/28b) surrounding one of the source/drain regions adjacent to the etching side (Fig. 1-6; col. 2, ln. 47 – col. 4, ln. 32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zheng et al. (US 6,762,085) in view of Yu et al. (US 20030222298).

Regarding claim 15, Zheng does not place any limits on the integrated circuits for which the MOSFETs of his invention may be used. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the MOSFETs of Zheng in any integrated circuit, including that of a memory cell circuit because Zheng does not place any limits on the integrated circuit for which the MOSFETs of his invention may be used and because memory cells having access transistors are well-known in the art. That being said, in the event that the MOSFET design of Zheng is applied to the creation of a memory cell, it is conventional in the art to form a bit line connected to the source/drain region of the transistor, as is shown by Yu (Fig. 4).

Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al. (US 6,777,298) in view of Oyamatsu (US 6,734,506).

Regarding claims 4 and 11, Roy discloses that the liner may be formed by oxidizing the gate but Roy does not specifically disclose that this oxidation process is a rapid thermal oxidation (RTO) process. Like Roy, Oyamatsu discloses a process of forming MOSFETs for use in an integrated circuit. Oyamatsu teaches that a gate can be oxidized to form an oxide layer on the sidewall thereof, by using a rapid thermal oxidation process (col. 6, ln. 66 – col. 7, ln. 8). At

the time of the invention, it would have been obvious to one of ordinary skill in the art to form the liner of Roy by using a rapid thermal oxidation process because Oyamatsu teaches that a RTO process can successfully oxide the sidewalls of a gate to form an oxide layer thereon.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roy et al. (US 6,777,298) in view of Yu et al. (US 20030222298).

Regarding claim 15, Roy states that his MOSFETs can be used in "any device with a PN junction" and does not place any limits on the integrated circuits for which the MOSFETs of his invention may be used. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use the MOSFETs of Roy in any integrated circuit, including that of a memory cell circuit because Roy states that his invention can be used in any circuit having a PN junction and because memory cells having access transistors are well-known in the art. That being said, in the event that the MOSFET design of Roy is applied to the creation of a memory cell, it is conventional in the art to form a bit line connected to the source/drain region of the transistor, as is shown by Yu (Fig. 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
April 27, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800